ION BEAM IRRADIATION EFFECTS IN KINTEX-7 FPGA RESOURCES

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Abstract. A comprehensive set of measurements has been pursued by our group to detect and characterize *Single Event Upsets* (SEUs) at the level of *configuration memory* (CRAM) and other logic resources on the chip such as *random-access memory* (BRAM) or user-accessible *Flip-Flop registers* (FFs). The device under study was a Xilinx Kintex-7 *Field Programmable Gate Array* (FPGA) build on TSMC's 28 nm technology node. Careful attention was given to the device behaviour when the integrity of its configuration memory was corrupted due to SEU occurrence. The device sensibility to its configuration corruption due to the SEU was further investigated employing SEM IP core as a primary mitigation solution for CRAM integrity. Both software and electrical parameters have been recorded with a custom-made radiation hardness qualification test bench. The SEU rates and cross-sections were determined based on data collected during test beam sessions using several ion species with different *Linear Energy Transfer* (LET).

Key words: FPGA, radiation hardness, online error mitigation, automatic test bench.

1. INTRODUCTION

In the recent years, the commercial *off-the-self* FPGAs have become a viable alternative to the *Application Specific Integrated Circuits* (ASICs) in co-processing hardware and front-end electronics for experiment-critical applications (*e.g.* high energy physics or astrophysics). With the caveat that they are more susceptible to radiation-induced effects than *radiation hardened by design* (RHBD) ASICs, the FPGAs offer many advantages like lowering the *non-recurring engineering* (NRE) costs, high parallelization of processing and flexibility in configuration allowing even partial reconfiguration while in operation. These characteristics are valid also for a low-price modern Static Random-Access Memory based FPGAs containing high logic density, *digital processing slices* (DSP) and *giga-bit transceivers* (GTX).

The radiation-induced effects represent a constant threat to the SRAM-based FPGAs reliability when they are used as part of a front-end hardware designed to operate in harsh environments with radiation background. Two distinct types of effects are known for perturbing the device functionality: the cumulative effects and *Single Event Effects* (SEE). The cumulative effects scales with the *Total Ionizing Dose* (TID) deposited into semiconductors active volume and *Displacement Damage* (DD), hence they manifest through an accelerated aging of the device with performance out of its nominal range up to complete loss of functionality.

For the current study we have focused on the effects in the SEE class, especially on SEU. This type of effects is triggered by a single high-Z energetic particle that traverses the active layers of the device giving rise along its path to a very localised and large charge deposit. Either primary high-Z particle or secondary ones produced through nuclear collision of a primary particle with semiconductor lattice might potentiate the probability of SEE occurrence, if deposited charge is at least equal to the critical charge of a given technology node [1]. There upon, charge generated along the path is collected by diffusion and might un-balanced a memory cells stored value by flipping the bit from one stabile state to the opposite one which means that a SEU occurred. A single high-Z particle may cause more than one semiconductor memory cell to be flipped when the deposited charge is shared between adjacent cells or the particle traverses these cells and the effect is called *Multi-Bit Upset* (MBU). Others SEE are more harmful inflicting a high current state on device as *Single Event Latch-up* (SEL) or destructive as *Single Event Gate Rupture* (SEGR) and *Single Event Burnout* (SEB).

Techniques to mitigate the radiation-induced SEEs represents a top priority and a continuous challenge for the software/hardware developers to make the SRAM-based FPGA design a viable solution for the radiation-hard systems. This paper presents an investigation of the radiation tolerance of a Kintex-7 FPGA through the induced effects in its firmware and electrical parameters. Various devices from Kintex-7 FPGA family have been also tested by other groups and the results are available in literature [2–7].

2. KINTEX-7 TEST BENCH AND IRRADIATION PROCEDURE

The *device under test* (DUT) evaluated by our group is a Kintex-7 FPGA part number XC7K70T. This is a lidless flip-chip packaged FPGA implemented in 28 nm *High K Metal Gate* (HKMG) technology featuring: 4,86 Mb of BRAM, 240 DSP slices, 65.6 k of logic cells as well as 8 GTX transceivers and other user logic resources [8]. The DUT flip-chip dice was thinned from 250 μm down to about 30–60 μm by removing through mechanical polishing the thermal interface material plus the substrate above the device semiconductor active volume. In total 6 samples have undergone this process and the thinned dice surface was mapped in a mesh of 16 × 16 points using an interferometer. The thinning was necessary to

ensure an optimal charge deposition at the level of the active layer of the electronics in ion beams with energy in the range of hundreds of MeV.

The custom test bench for irradiation was designed around the Kintex-7 test board having the minimal number of components required to ensure the FPGA basic operation. The FPGA was configured to work in JTAG mode without any external configuration FLASH memory on the board. This design was chosen to prevent failures of electronic components near DUT and thus influencing the measurements. The DUT was powered over a 5 m screened multi-core cable from a power management unit based on ADP5050 integrated circuit and controlled by a custom *data acquisition system* (DAQ). The power management unit has 6 power rails suppling the DUT which are monitored continuously by the DAQ system, while the current measurement circuitry is inherited from the test bench described in detail here [9]. Further, the sampled values of the power consumption on each rail are sent to a PC where they are displayed in a LabVIEW *graphical user interface* (GUI) and saved within ASCII files every 50 ms. The FPGA power sequencing and power cycling are also foreseen in the DAQ's firmware, while the voltage drops along the multi-core cables are overcome by placing the DC-DC converters feedback sense near the FPGA. The DUT programming and blind scrubbing are done *via* Xilinx JTAG Programmer located 1.5 m away from the FPGA. Firmware status is checked with a NEXYS3 FPGA development board that is connected also to the PC from the experimental room. A second LabVIEW GUI has been implemented to control and communicate with NEXYS3 development board while the firmware status is saved in the second ASCII file. More details about the test bench components and characteristics are given in reference [10].

The firmware for DUT plays a crucial role when FPGA's logic resources and CRAM are tested against radiation-induced SEE. Our group adopted a straight forward solution to implement multiple versions of firmware that allows the evaluation of SEU occurrence rate *versus* LET for CRAM, BRAM and *Flip-Flops* (FFs). Two FPGAs with the dice thinned in the range 45–55 μm were characterised during beam tests at the following irradiation facilities: *Heavy Ion Facility* (HIF) from *Universite Catholique de Louvain* (UCL) in Belgium [11] and SIRAD facility from *Legnaro National Laboratories* (LNL) in Italy [12]. Table 1 summarizes the parameters of the ion beams to which the DUT was exposed during SEU measurements.

Table 1

Ion beams used in SEU rate measurements

Facility	**Ion species**	**Energy [MeV]**	**Effective LET [MeV·cm^2/mg]**	**LET uncertainty [MeV cm^2/mg]**
HIF	^{22}Ne	237	3.660	± 0.122
SIRAD	^{16}O	108	3.785	± 0.292
	^{19}F	118	5.334	± 0.481
	^{28}Si	157	13.354	± 0.324

All the measurements have been performed with the DUT surface at normal incidence with the ion beam longitudinal axis. The LET uncertainty is given by the thinned dice surface asperities. The effective LET value in case of 45 μm dice thickness and 55 μm were determine by simulating 1000 events in Silicon for each of the above ions species with the SRIM/TRIM software (*Stopping and Range of Ions in Matter*) [13]. Other sources of uncertainty in the beam parameters are induced by the flux variation which was 5% at HIF facility, while 20% at SIRAD. At both facilities the irradiation was performed in vacuum and beam fluxes ranged from 100 ions/(cm^2 s) up to 1200 ions/(cm^2 s).

3. DATA ANALYSIS AND RESULTS DISSEMINATION

Given the increased SRAM capacity on the device, the *configuration memory* (CRAM) is physically embedded in blocks tiles on the device and logically organised in frames of 101 words 32-bit length [14]. For diminishing SEU occurrence in adjacent memory cells leading to MBU in the same frame, the bits of CRAM words are physically interleaved to improve the efficiency of *error correcting codes* (ECC) and *single-error correct/double-error detect* codes (SECDED) [15]. Our DUT has 18884576 bits [8] of configuration memory which are set according to the user design.

The corruption mitigation of CRAM bits is prioritised according to the Xilinx concept of essential bits for maintaining DUT functionality. The hierarchy of priorities from lowest to highest are device configuration bits, essential bits, prioritized essential bits and critical bits (see [16] for further details). Keeping the CRAM integrity is vital in radiation environments where SEU occurrence probability is high considering that such events are responsible for changing the FPGA programming, also random switching the interconnections by affecting the so called “switching matrix” between the *configuration logic blocks* (CLBs) and also device I/O blocks.

Initially, we irradiated two FPGA samples without any CRAM scrubbing solution, just reconfiguration through a JTAG programmer. The first DUT was programmed with a firmware enabling about 1% of the FFs (as detailed in [10]) and the device was irradiated with a ^{19}F ion beam to a cumulated fluency of 6.7×10^6 ions/cm^2. For the second DUT another firmware was used implementing a chain of single-voted FFs which enabled 40% from the total of 82000 FFs available on the device. This time the DUT was irradiated with a ^{22}Ne ion beam to fluency 14.3×10^6 ions/cm^2. The effect of the irradiation was the loss of DUT functionality because of CRAM corruption correlated with a high-current state in the power rail suppling the FPGA core and BRAM as seen in figure 1. The first DUT after configuration sink around 400 mA on the core power rails, where σ_{Icore} ±1 mA and σ_{Vcore} ±1 mV. As SEU and MBU affect the CRAM integrity,

unused logic resources are introduced into and around the user defined logic architecture. This leads to considerable increase of current consumption since the number of enabled logic resources grows. The current consumption saturates at 3.5 A due to power supply limitation. The same behaviour is observed for the second DUT. When the device is reconfigured without power cycling the current consumption it returns to nominal values, a clear proof that no SEL occurred.

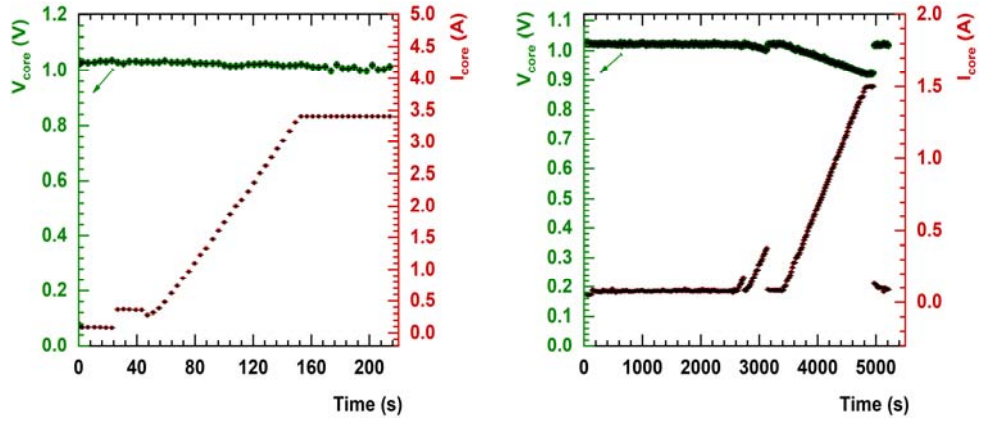

Fig. 1 – (Color on-line) Core current increasing during exposure in ^{19}F beam (left side) and ^{22}Ne beam (right side). The saturation in DUT power consumption corresponds to loss of device functionality due to CRAM corruption.

The assumption made by us is that the I_{core} slope value is correlated with the beam flux, LET of beam particles, device temperature and firmware occupancy on CRAM. However, this hypothesis should be proved and parametrized. In support for this assumption, we made a thermal stress test on the device. The device was configured, and the test was started at room temperature by externally heating the FPGA dice up to 90^0 while monitoring its power consumption. The core power consumption was sampled at each 100 ms and the temperature measured from time to time with the device built in thermal diode. Test results highlight a strong correlation between device dice temperature and I_{core} current, see figure 2.

As a main mitigation solution for SEU in CRAM we decided to embed in our firmware versions the Soft Error Mitigation core (SEM IP) [17]. This is a free pre-verified solution made available by Xilinx which allows CRAM scrubbing. The SEM IP core can detect, correct and classify CRAM bits which are affected by SEU or MBU. The core can be switched in an idle state for error injection to a specific CRAM bit location. Error injection tests without beam and measurements in ion beams revealed also high current jumps caused just by flipping a single bit into CRAM. The FPGA behaves as if its logic resources are randomly interconnected. The FPGA fully recovers immediately after the SEM IP detects and corrects the faulty bits [18].

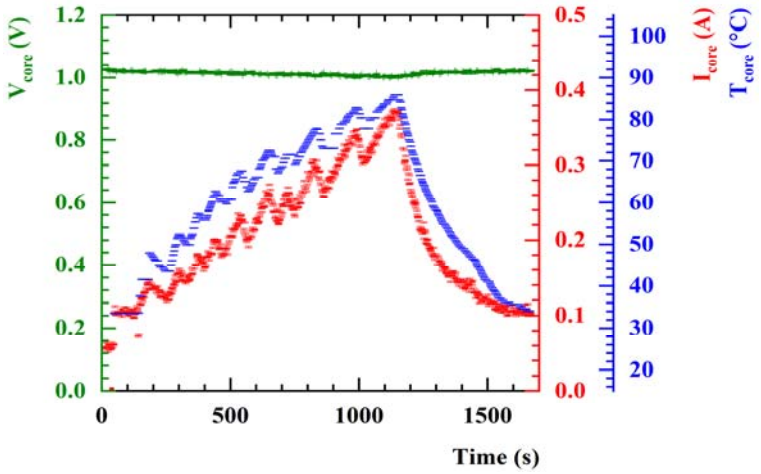

Fig. 2 – (Color on-line) Kintex-7 core current consumption *versus* its dice temperature.

Reports from SEM IP core were dumped to an ASCII file during irradiation. They allowed the determination of the SEU rate in the device CRAM for each specific LET value. We observed that the detection and correction efficiency of the SEM IP core quickly diminishes as the ion LET or ion flux increases, scaling further down with growing numbers of essential and critical bits in the programmed firmware. For the cross-section calculation per CRAM bit we considered just the sequences from an irradiation run with SEM IP execution time below 5 s. For a larger execution time the SEM IP usually failed or uncorrected MBU occurred even for beam fluxes in order of 100 ions/(cm^2 s). In the case of ^{16}O ion beam we determined a SEU cross-section of (68.5 ± 5.94) × 10^{-11} cm^2/bit at LET of (3.785 ± 0.292) MeV·cm^2/mg, while for ^{28}Si ion beam the SEU cross-section is (22.3 ± 2.26) × 10^{-10} cm^2/bit at LET of (13.354 ± 0.324) MeV·cm^2/mg. These cross-section values plus the one measured for the ^{22}Ne ion beam are shown in figure 3 and they are found in agreement with similar measurements in literature [5, 19].

Resilience of the BRAM against SEU was investigated using the SEM IP core and a dedicated firmware with BRAM18 and BRAM36 built-in memory blocks. The firmware had a very low occupancy with 0.87% of essential bits from CRAM size. A fix pattern of bits was hardware coded into the devices BRAM and downloaded into ASCII file as reference before the DUT was irradiated. During exposure the SEM IP report was closely monitored to eliminate duplicates of error detection and incomplete reports due to SEM IP crashes. After irradiation the BRAM contents was dumped into an ASCII file and analysed using LabVIEW. The SEU cross-section per BRAM bit obtained in beams of ^{16}O and ^{28}Si are shown in figure 4.

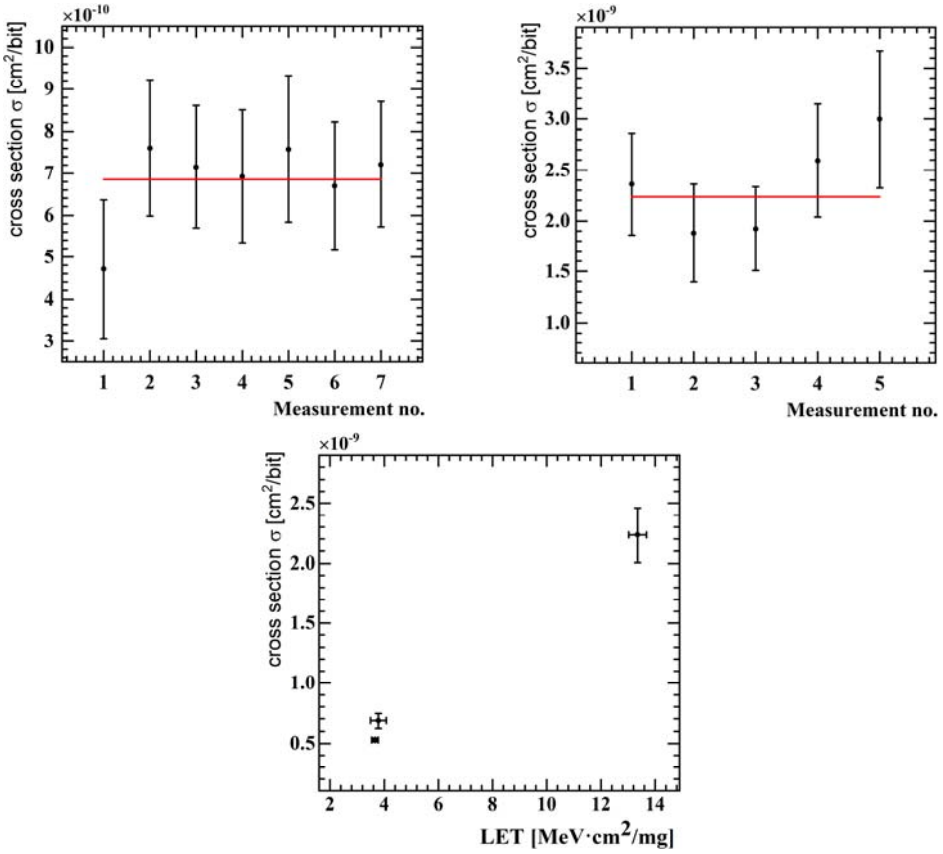

Fig. 3 – (Color on-line) The cross-section measurements for SEU per CRAM bit in ^{16}O (top left), ^{28}Si (top right) ion beams. The bottom plot shows the cross-section values with respect to LET for ^{16}O, ^{28}Si and ^{22}Ne.

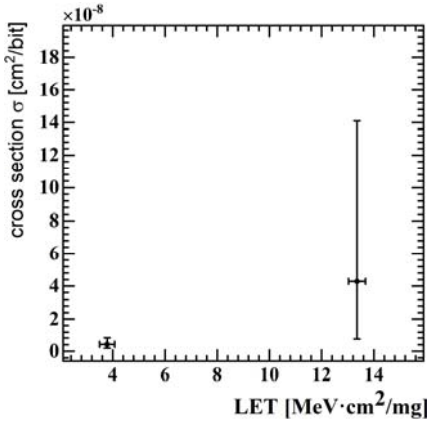

Fig. 4 – Cross-section per BRAM bit *versus* LET.

For ^{16}O ion beam the measured BRAM cross-section value of $(0.42^{+0.392}_{-0.228})\times10^{-8}$ cm^2/bit at LET of (3.785± 0.292) MeV·cm^2/mg is in agreement with the literature [5, 19]. A higher cross-section value is obtained for ^{28}Si ion beam $(4.285^{+9.81}_{-3.54})\times10^{-8}$ cm^2/bit at LET of (13.354± 0.324) MeV·cm^2/mg, but with a large uncertainty due to poor statistics which accommodate the value quoted in literature [5, 19].

The FFs radiation tolerance was evaluated with a firmware enabling a chain of Flip-Flops with a *Triple Modular Redundancy* (TMR) architecture and SEM IP. In total 20% of total FFs were used and the essential bits percentage was kept close to 7% of the total available in CRAM. The DUT programmed with the FF-based firmware was exposed successively to ^{16}O, ^{28}Si and ^{22}Ne ion beams. A well-defined 32-bit pattern was shifted by the FFs chain and the output read and compared by Nexys-3 development board. Then the result was saved into an ASCII file for later analysis. The number of detected SEU was determined by taking into consideration the changes in several flags from the saved ASCII file. Five measurements have been carried out with ^{16}O ion beam and the calculated cross-section is of (38.11 ± 5.73) × 10^{-10} cm^2/FF at LET of (3.785 ± 0.292) MeV·cm^2/mg, see figure 5 left-side plot. The measured SEU cross-section per device FF with respect to the LET of ions is shown in the right-hand side plot of figure 5.

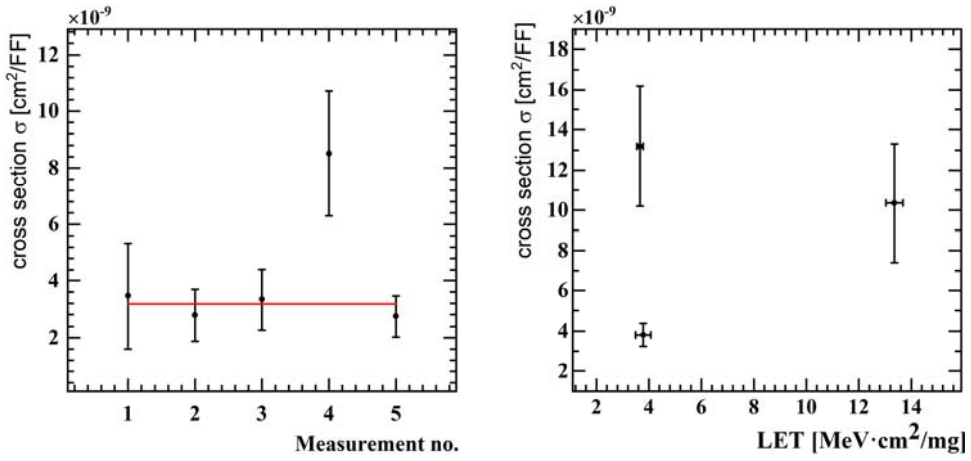

Fig. 5 – (Color on-line) The cross-section measurements for SEU FF in ^{16}O (left side), while the right-side plot shows the cross-section values with respect to LET for ^{16}O, ^{28}Si and ^{22}Ne.

These values do not agree with other published measurements [5] because our determinations were mostly dominated by dynamic effects, *e.g. Single Event Transient* (SET), and SEU in CRAM randomly affecting the FF chain until SEM IP correction occurred. Also, the cross-sections measured for ^{28}Si and ^{22}Ne ion beams have great uncertainties due to low statistics which could be gathered during very

limited beam-time. Generally, a static method is adopted for testing FF radiation hardness. It implies that the FF chain is instantiated with a fixed logic and no clock source is present during irradiation. Then after exposure, the FF chain data is downloaded and compared to its initial pattern.

4. CONCLUSIONS AND PLANS

SEU and MBU phenomenon could have harmful consequences when occurring in SRAM-based FPGA configuration memory leading to system malfunction and overloading the power budget of the application, especially in big detectors where large numbers of such devices are used. CRAM scrubbing and partial reconfiguration are successfully solutions for mitigating these effects unless a SEL takes place and the device requires power-cycling to recover. The SEU cross-section corresponding to several values of the incident ion LET have been measured for CRAM and BRAM bits, and FF registers. Work is in progress to investigate DUT behaviour in higher LET events and determine the SEU cross-sections for each logic resource on the device.

We have measured the SEU cross-section in CRAM with ^{28}Si ion beam as being $(22.3 \pm 2.26) \times 10^{-10}$ cm^2/bit at LET of (13.354 ± 0.324) MeV·cm^2/mg. This value can be further used to check the number of SEUs occurring in CRAM through secondary ionization in hadron beam irradiation. Therefore, the recoiling ion which originates from the interaction of high energy hadrons with device silicon lattice triggers a SEU.

These results will allow us to extrapolate the Kintex-7 performance for the high energy physics detectors working in mixt-field radiation environments. Relying on performed radiation hardness tests the Kintex-7 FPGA is a promising solution to be considered for digital part architecture of detector front-end electronics.

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REFERENCES

1. C. Detcheverry *et al.*, *SEU critical charge and sensitive area in a submicron CMOS technology*, IEEE Transactions on Nuclear Science **44**, 2266–2273 (1997).
2. L. Harten *et al.*, *Necessity of Fault Tolerance Techniques in Xilinx Kintex 7 FPGA Devices for Space Missions: A Case Study*, Euromicro Conference on Digital System Design (DSD), Vienna, Austria (2017).

3. G. Swift, *Micro-Latchup in 7-Series FPGAs and Other Ongoing XRTC Investigation*, Single Event Effects (SEE), Symposium San Diego, USA (2015).
4. M. Cannon *et al.*, *Evaluating Xilinx 7 Series GTX Transceivers for Use in High Energy Physics Experiments Through Proton Irradiation*, IEEE Transactions on Nuclear Science **62**, 2695–2702 (2015).
5. D.S. Lee *et al.*, *Single-Event Characterization of the 28 nm Xilinx Kintex-7 Field-Programmable Gate Array under Heavy Ion Irradiation*, Radiation Effects Data Workshop (REDW), Paris, France (2014).
6. D.M. Hiemstra, V. Kirischian, *Single Event Upset Characterization of the Kintex-7 Field Programmable Gate Array Using Proton Irradiation*, Radiation Effects Data Workshop (REDW), Paris, Franc (2014).
7. K.M. Sielewicz *et al.*, *Experimental methods and results for the evaluation of triple modular redundancy SEU mitigation techniques with the Xilinx Kintex-7 FPGA*, IEEE Radiation Effects Data Workshop (REDW), New Orleans, USA (2017).
8. Xilinx 7 Series FPGAs Data Sheet: Overview, DS180 (v2.5). Available online (last accessed April 10, 2018).
9. V.M. Placinta *et al.*, *Test Bench Design for Radiation Tolerance of Two ASICs*, Romanian Journal of Physics **62**, 903 (2017).
10. L.N. Cojocariu *et al.*, *Monitoring system for testing the radiation hardness of a KINTEX-7 FPGA*, AIP Conference Proceedings **1722**, 140009 (2016).
11. G. Berger, G. Ryckewaert, *The heavy ion irradiation facility at CYCLONE – a dedicated SEE beam line*, IEEE Radiation Effects Data Workshop (REDW), Indian Wells, USA (1996).
12. D. Bisello *et al.*, *The SIRAD irradiation facility at LNL*, Proceedings of Ion Beams 12th Conference, Laboratori Nazionali di Legnaro, Padova, Italy (2012).
13. SRIM/TRIM – The Stopping and Range of Ions in Matter. Available online (last accessed April 9, 2018).
14. Xilinx 7 series FPGAs Configuration user guid, UG470 (V1.11). Available online (last accessed April 10, 2018).
15. M. Wirthlin *et al*., *A Method and Case Study on Identifying Physically Adjacent Multiple-Cell Upsets Using 28-nm, Interleaved and SECDED-Protected Arrays*, IEEE Transactions on Nuclear Science **61**, 3080–3087 (2014).
16. Soft Error Mitigation Using Prioritized Essential Bits, XAPP538 (v1.0). Available online (last accessed April 10, 2018).
17. Soft Error Mitigation Controller, LogiCORE IP Product Guide PG036 (V4.1). Available online (last accessed April 11, 2018).
18. V. M. Placinta, L. N. Cojocariu, *Radiation Hardness Studies and Evaluation of SRAM-Based FPGAs for High Energy Physics Experiments*, PoS TWEPP-17, Santa Cruz, USA (2018).
19. M. J. Wirthlin *et al.*, *Soft error rate estimations of the Kintex-7 FPGA within the ATLAS Liquid Argon (LAr) Calorimeter*, Journal of Instrumentation **9**, C01025 (2014).
20. LHCb Upgrade – Particle Identification TDR, LHCb-TDR-014. Available online (last accessed April 11, 2018).