

## AN QPSK 3G TRANSMITTER BASED ON THE TMS320C6711DSP\*

C. T. ANGELIS<sup>1,2</sup> and A. LAMBROS<sup>2</sup>

<sup>1</sup> Department of Physics, University of Ioannina, 45110 Ioannina, Greece, kaggelis@cc.uoi.gr

<sup>2</sup> Department of Communications, Informatics and Management, TEI of Epirus, 47100 Arta, Greece, e-mail: lambros@auth.gr

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In this paper, we design and implement a QPSK 3G Transmitter based on a Digital Signal Processor, from the Texas Instruments 320C67x DSP family.

The paper first describes the basics of the 3G Quadrature Phase Shift Keying (QPSK). The transmitter implementation is presented in detail next, along with the simulation results with regards to the performance and complexity associated with such a flexible implementation.

The obtained overall performance is analyzed, along with the flexibility of the software approach, which makes the proposed DSP based transmitter implementation effective for 3G radio applications, where state of the art performance, size and weights are critical aspects with respect to hardware complexity or cost.

*Key words:* SDR, QPSK, 3G.

### 1. INTRODUCTION

During the last few years, cellular digital communication systems have grown dramatically fast. Among different configurations used all over the world, 3G wireless communications is the next phase in wireless communications that offers wideband data services and multimedia wideband products and services. A new challenge to the mobile communication industry is the integration of multiple systems and applications on a single mobile device. Also the increasing demands for multimedia applications and other services with high data rate, without a corresponding increase in RF spectrum allocation motivates the need for new techniques to improve spectrum utilization that do not require more bandwidth and network capacity [1]. With the emergence of new standards, programmable devices that consume minimum power are in demand. The major predicament with programmable devices, such as high performance programmable digital signal processor (DSP) solutions, is that they consume more power compared to hard-wired chips. SWR techniques aim at performing as much as

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possible processing in digital and particularly in software by moving the digital to analog conversion (DAC) as close as possible to the antenna. That led to extensive research on 3rd generation mobile communications, such as WCDMA and cdma2000.

In this paper a simple design method is presented for a low cost SDR transmitter as well as computer simulation results of the overall performance in terms of signal quality and speed of execution on the DSPs. The scope of this study is restrained to the digital implementation of the modulation blocks of a WCDMA transmitter. After a precise description of our software radio (SWR) platform, the information necessary to make a digital implementation of WCDMA modulator is given. The analysis showed that this increasingly digital approach is now feasible, even for 3G waveforms as WCDMA, with current technology at least for infrastructure equipment.

## 2. TRANSMITTER DESIGN

The block diagram in Fig. 1 shows the physical architecture of the proposed super-heterodyne design QPSK modulator. In this architecture, the complex baseband data is filtered, in order to avoid the intersymbol interference and promptly converted to an analog signal. After the DAC, the signal is passed through a quadrature modulator (RF Section), which may then continue on to several stages of mixers and filters to reach the desired radio frequency. The performance of the quadrature modulator is especially critical when looking at the error vector magnitude (EVM) of the transmitted signal. A simple digital correction circuit will remove constant amplitude and phase error. Should the errors vary with frequency, a much more complicated correction system is required. The advantage of this architecture is that the DACs only need to sample at the bandwidth of the signal so higher data rate signals may be generated.

The proposed transmitter is divided into 2 sections, the digital section, which is implemented in the DSP, and the analog RF section. The core of our

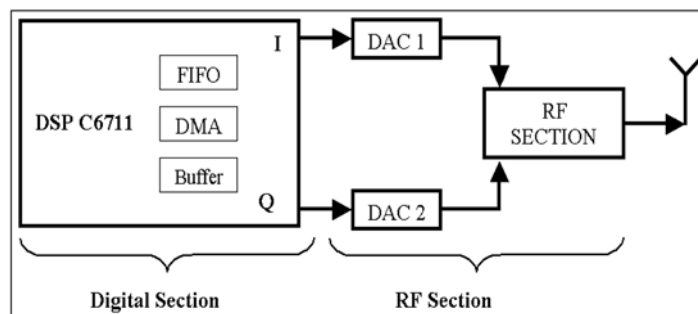


Fig. 1. – Block diagram of the proposed QPSK transmitter.

SWR platform is a-DSP board based on last generation VLIW processor (TIC6711 at 200 MHz) [2] that permits very fast execution of high-level language programs. It has a modular hardware architecture making future upgrades possible. This platform permits to study the interactions and behavior of the various entities in a cellular network when reconfiguration of the air interface occurs. Currently, all code development is done in C, enabling portability from this platform to any other processor, as the SWR dogma requires. The price for portability is a limitation on execution speed, depending on the quality of the associated software tools (*i.e.* the C compiler). The interface of this board with the analog world is via a wideband transmitter (Tx) module based on wideband D/A components. Module parameters are fully software controlled and their principle of operation is described next.

The digital segment of the transmitter generates the baseband transmit signal by modulating an input data burst according to the selected communication standard. The baseband QPSK is performed digitally by multiplication of the I and Q data stream by digitally generated (sampled) cosine and sine waves of the programmed carrier frequency. As it is known, the sampling frequency is a software controlled parameter and can be realized either by the DUC or by software in the DSP. In our survey we chose to realize the carrier by software in order to increase the reconfigurability and reconfiguration that SWR needs.

The hardware structure, which is appropriate to implement the functionality of a digital transmitter, is the TMS320C6711. The Texas Instrument's TMS320C6711 DSP Processor [3] is used for high-performance DSP multichannel and multifunction applications due to the high-performance, advanced Velocity™ very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI).

The chosen modulation is based on QPSK. QPSK is a bandwidth efficient modulation scheme. As compared to the BPSK modulation scheme, QPSK gives the same BER performance but carries twice the data rate in the same bandwidth. The implementation of modulation and demodulation is simple, and, therefore, QPSK is very attractive for use in wireless communications. The phase of a QPSK signal can take one of four possible values. The four values are equally spaced. They are practically chosen to be 45°, 135°, 225° and 315°. For a symbol interval, the so-called  $\pi/4$ -QPSK can be mathematically represented by [4]:

$$S_{QPSK}(t) = I_{QPSK}(t) \cos[2\pi f_c t] - Q_{QPSK}(t) \sin[2\pi f_c t] \quad (1)$$

where  $A$  is signal amplitude and  $f_c$  the carrier frequency.

The direct ( $I$ ) and quadrature ( $Q$ ) components of the signal are defined as

$$I_{QPSK}(t) = A \cos[\theta_i(t)] \quad (2)$$

$$Q_{QPSK}(t) = A \sin[\theta_i(t)] \quad (3)$$

The  $I$  and  $Q$  components are baseband signals that ease the simulation.

According to the specification of W-CDMA, a root raised cosine filter with a roll-off factor of  $a = 0.22$  is used for pulse shaping. The pulse shaping reduces the intersymbol effects and the spectral bandwidth of baseband signals. The roll-factor of the filter is 0.22. Its impulse response is [4]:

$$h(t) = \frac{4a}{\pi} \frac{\cos\left(\frac{\pi t(1+a)}{T_s}\right) + \frac{\sin\left(\frac{\pi t(1-a)}{T_s}\right)}{\frac{\pi t}{T_s}}}{1 - \left(\frac{4at}{T_s}\right)^2} \quad (4)$$

This pulse shaping is a global Nyquist filtering distributed between the transmitter and the receiver, suppressing that way the inter symbol interference on the complete system chain.

The baseband processing functional configuration includes several steps. At the beginning Data Randomization, through a modulo-2 addition between the information serial data stream and a pseudo-noise sequence, has been adopted to grant appropriate energy dispersal to the transmitted signal. The channel encoding process, to ensure enough error protection against channel degradations, is based on a mother Convolutional code 1/4. In order to guarantee maximum system flexibility a Puncturing procedure has also been inserted allowing a trade off between net data rate and channel quality. Applying a Time Interleaving process to the transmitted data reduces the probability of a burst error event, so maximizing the Convolutional code performance. From each encoded couple of bits a complex QPSK (Quaternary Phase Shift Keying) symbol is generated. The following processing block is the Frequency interleaving to allow effective frequency diversity. A Differential Modulation algorithm comes next, obtaining a  $\pi/4$ -shift D-QPSK; by the use of this mapping method of data bits, the receiver architecture is simplified as it does not need to implement channel estimation and equalization.

As was mentioned before, the DSP processing board interfaces to the analog world through a mezzanine card of digital to analog conversion. In this card there are two wideband ADCs components for the  $I$  and for the  $Q$  channel. The DAC generates the modulated signal at an intermediate frequency that is then converted to the RF. Continued improvements in DACs should eventually allow the IF to be moved up sufficiently to eliminate an entire mixer stage.

In our design we used the AD9777 DAC [5], from Analog Devices, with 16-Bit Resolution and 160 MSPS/400 MSPS Input/Output Data Rate. The AD9777 features a serial port interface (SPI) that provides a high level of programmability, thus allowing for enhanced system level options. These options include

selectable  $2 \times / 4 \times / 8 \times$  interpolation filters;  $f_S/2$ ,  $f_S/4$ , or  $f_S/8$  digital quadrature modulation with image rejection; a direct IF mode; programmable channel gain and offset control; programmable internal clock divider; straight binary or twos complement data interface; and a single-port or dual-port data interface [5].

The RF section consists of the AD8349 QPSK modulator from Analog Devices [6]. The AD8349 RF quadrature modulator can be used as a direct-to-RF modulator in digital communication systems such as GSM, CDMA, and WCDMA base stations, and QPSK or QAM broadband wireless access transmitters. The AD8349's excellent phase accuracy and amplitude balance enable high performance direct RF modulation for communication systems. The differential LO input signal is buffered, and then split into an in-phase (I) signal and a quadrature-phase (Q) signal using a polyphase phase splitter. These two LO signals are further buffered and then mixed with the corresponding I channel and Q channel baseband signals in two Gilbert cell mixers. The mixers' outputs are then summed together in the output amplifier. The output amplifier is designed to drive 50 loads. The RF output can be switched on and off within 50 ns by applying a control pulse to the ENOP pin [6].

The AD8349 can be divided into five sections: the local oscillator (LO) interface, the baseband voltage-to-current (V-to-I) converter, the mixers, the differential-to-single-ended (D-to-S) amplifier, and the bias circuit [6]. A detailed block diagram of the device is shown in Fig. 2. The LO interface generates two LO signals at 90 degrees of phase difference to drive two mixers in quadrature. Baseband signals are converted into currents by the V-to-I converters, which feed into the two mixers. The outputs of the mixers combine to feed the differential-to-single-ended amplifier, which provides a 50 output interface. Reference currents to each section are generated by the bias circuit. Additionally, the RF output is controlled by an output enable pin (ENOP), which is capable of switching the output on and off within 50 ns.

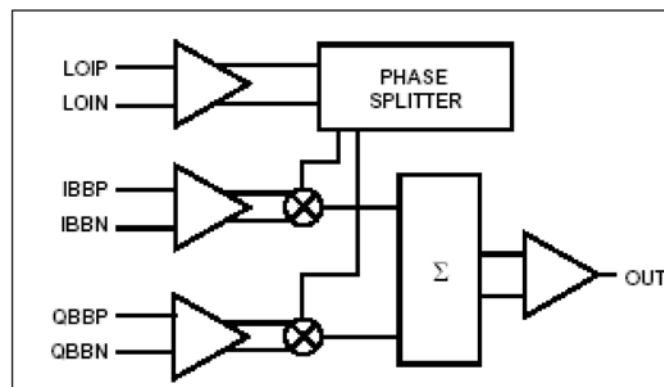


Fig. 2. – Block diagram of the AD8349 RF quadrature modulator.

### 3. RESULTS AND DISCUSSION

Performance in terms of both quality of the transmitted signal, and of computation speed is considered here.

Before implementing the QPSK Transmitter on the DSP based hardware platform, a simulation was performed on a PC. This was useful for rapid testing of implementation alternatives and in order to avoid errors in the final implementation. The simulation was programmed in the MATLAB language. The Baseband QPSK signal generated in MATLAB with final carrier frequency of 40 kHz. All the necessary steps to produce the Baseband QPSK signal mentioned before, *i.e.* Data Randomization, channel encoding, Time Interleaving and finally Differential Modulation algorithm for obtaining the  $\pi/4$ -shift D-QPSK were performed through software in order to insure the maximum reconfigurability needed in SDRs. The resulting Baseband QPSK signal in the time domain is shown in Fig. 3.

The MATLAB code after the simulation was compiled in C language. The assembly code generated from the C program became the foundation for the optimized system implementation on the TMS320C6711.

In order to test the design, we sent the raw data to the host PC, saved the data in a file, and plotted the data with Matlab. The raw data was successfully downsampled and acquired by the DSP board and sent to the PC. Fig. 4 shows

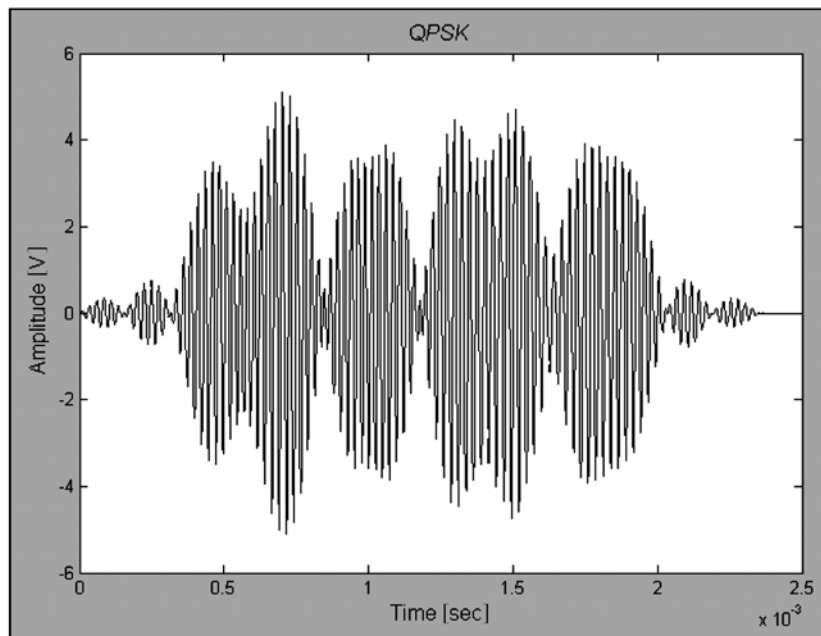


Fig. 3. – The Baseband QPSK signal with carrier frequency 40kHz for random data.

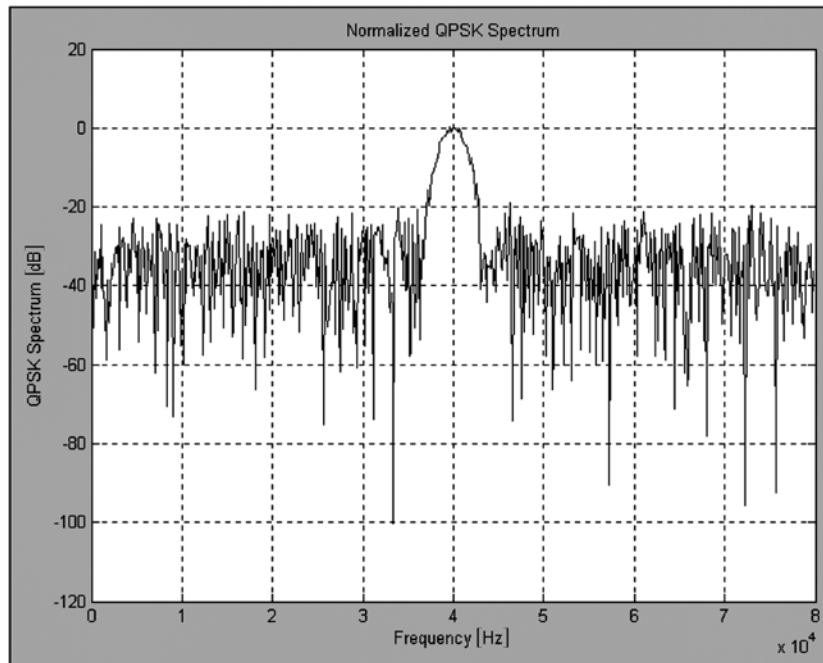


Fig. 4. – Normalized Baseband QPSK spectrum with carrier frequency 40 kHz.

the Normalized Baseband QPSK spectrum as it was calculated in the output of the DSP. The digital baseband QPSK signal is centered at the 40 kHz carrier frequency. The background noise is inserted due to the RTDX procedure, which was chosen for the measurement.

After this test the baseband digital QPSK signal was sent to the AD8349 RF quadrature modulator board through the two AD9777 wideband D/A components. The RF modulator was tested using a spectrum analyzer. The spectrum data were sending back to the PC and plotted with Matlab. The final spectrum is shown in Fig. 5. The analog RF QPSK signal is centered at the 2 GHz carrier frequency. The background noise is inserted due to the digital to analog procedure and due to the RF board, which was chosen for the RF modulation.

During the implementation procedure were also obtained several performance measurements in terms of execution speed (CPU cycle counts) and attained bit rates on the TMS320C6711 DSP at 200 MHz. We measured the global performance of the total baseband transmit chain which of Bit Generation, baseband QPSK modulation and IO Data Transfer. The attained chip rate performance for the modulation procedure only is 1840 kbit/s while the theoretically required is 3840 kbit/s for both modulation and demodulation at the same time. These measurements indicate that a single C6711 could handle the baseband QPSK modulator to run in real-time and deliver acceptable real-time performance.

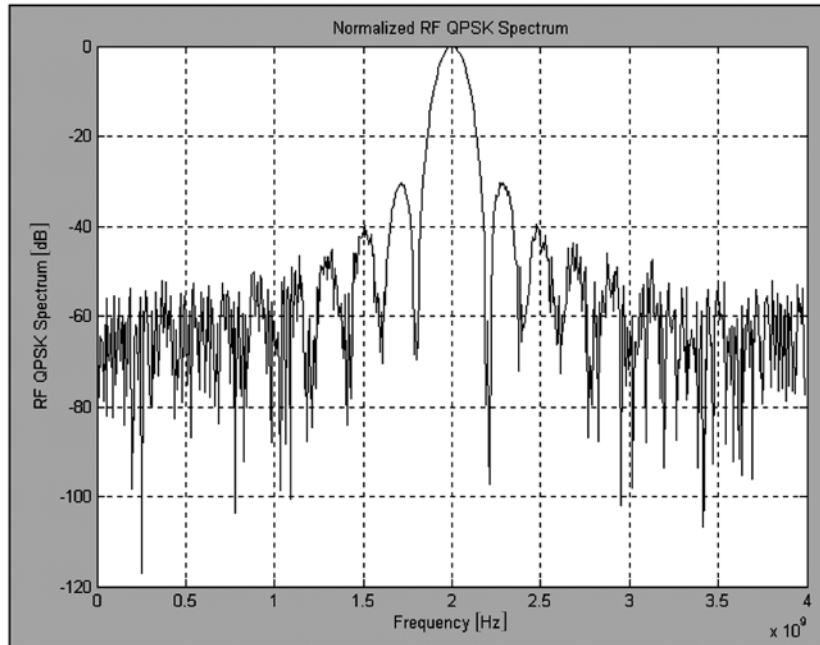


Fig. 5. – The Normalized spectrum of the QPSK modulated transmit RF signal with carrier frequency 2 GHz.

However it must be noted that currently the C6x DSP chip is not destined to commercial mobile terminals due to its high power consumption, size and price.

#### 4. CONCLUSIONS

In this paper it was presented how the software radio concept was effectively used to build a low cost WCDMA modulator. For this, a DSP-based QPSK transmitter has been simulated and implemented on the TMS320C6711 Floating-Point DSP. The whole system consists of a DSP core implemented on the board, a wideband digital to analog board and an RF QPSK transmitter. Results shown that the DSP is capable to manipulate through signal processing the Bit Generation, baseband QPSK modulation and IO Data Transfer in real time.

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